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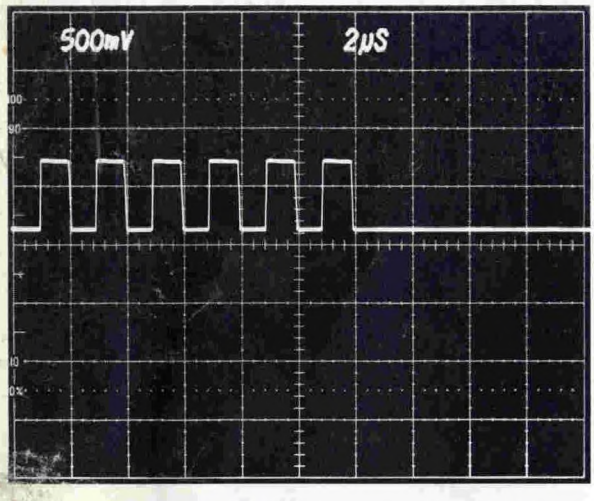
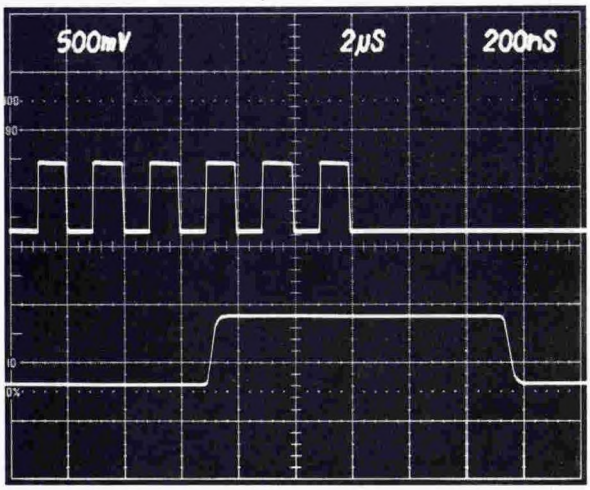
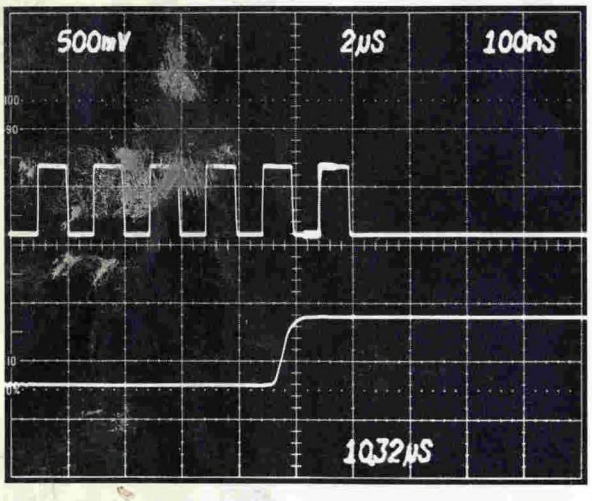
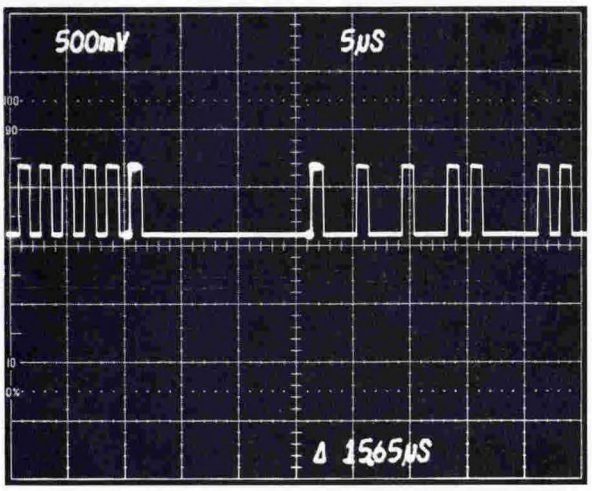
# TEKSCOPE

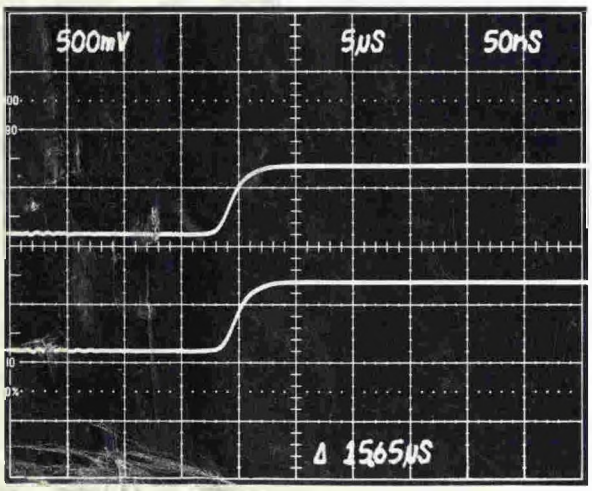
Volume 8 Number 1 1976

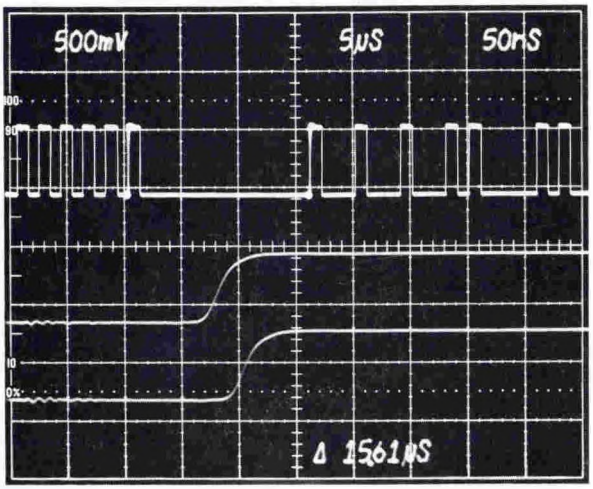


# TEKSCOPE

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Editor: Gordon Allison

## Contents



**Cover:** These photos show the versatility of the new 7B85/7B80 time base combination. The display at lower right shows a △ time measurement being made while viewing the main sweep and both delayed sweeps simultaneously. Digital readout of △ time is at the bottom of the display.



Paul Farley Les Larson Bruce Hofer

# △ Time measurement for the 7000 Series

Time measurements are often made with an oscilloscope—measurements of rise time, pulse width, time between pulses, etc. They are relatively easy to make once you are familiar with the instrument and are typically accurate to within 2%. Some time measurements can be made more accurately by using a delaying sweep, but until recently these have been relatively time-consuming and subject to operator error.

Delaying sweep measurements using the 10-turn Delay Time Multiplier (DTM) typically are accurate to about 1% or better. The technique involves positioning the starting point to a reference graticule line with the DTM, noting the control setting, then rotating the DTM to position the stopping point to the reference line and again noting the control setting. The difference between the two readings is multiplied by the main time base setting to get the time difference.

Making delay measurements became considerably faster and easier with the introduction of the TEKTRONIX DM40 and DM43 Digital Multimeters for the 400-Series Portable Oscilloscopes. In these instruments, the Delay Time Multiplier is replaced by an uncalibrated control called Delay Time Position and a 3½-digit LED readout. Delay measurements are made by selecting the first of two points with the Delay Time Position control, zeroing the meter, then setting the Delay Time Position control to the second point. The time delay is read out directly on the digital display. No calculations are necessary. The DM40 and DM43 offer more resolution and accuracy than the 10-turn dial, primarily for time intervals less than 1/10 of the delay range used.[1] And the direct readout of delay time greatly reduces the possibility of error.

Now two new time bases for the 7000-Series Oscilloscopes offer new ease and accuracy for making delay measurements. The 7B85 Delaying Time Base and its companion 7B80 Time Base are designed primarily for

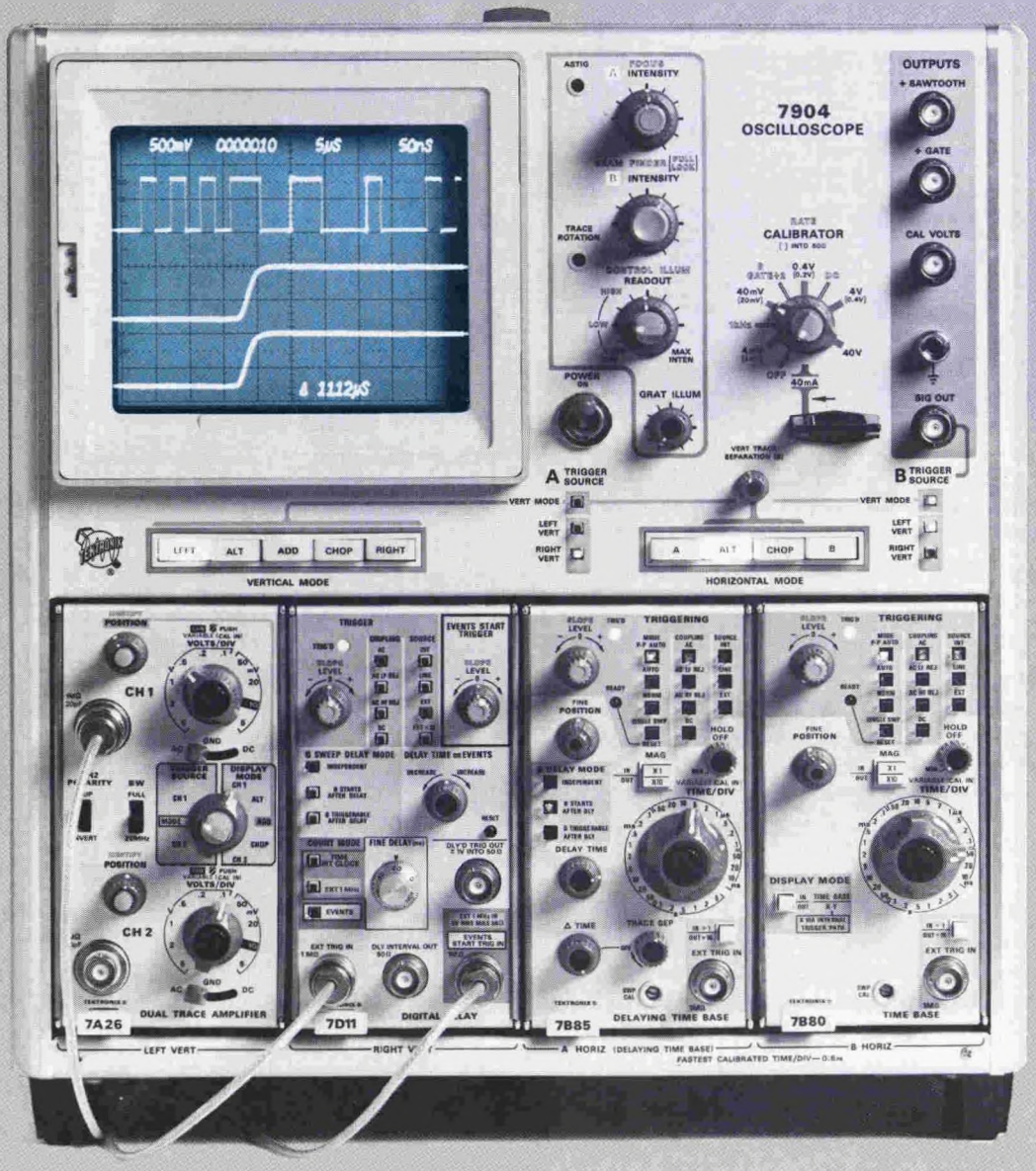
use with the 7700, 7800, and 7900 Series instruments. They offer improved performance in every characteristic over the 7B70 and 7B71 (which they replace). Since we have been discussing delaying sweep measurements, let's examine this capability first.

**△ (delta) delay time mode**

In the 7B85, the conventional Delay Time Multiplier control is replaced by two controls labeled DELAY TIME and △ TIME. A third control enables the △ time function and provides trace separation (fig 1).

The DELAY TIME control is used to make time measurements from sweep initiation to some point on the trace. The delay time (the time from the start of the main sweep to the beginning of the intensified zone) is digitally computed and displayed as a 4-digit number on the lower line of the crt.

To make time measurements more accurately and conveniently between any two points on a waveform, you can switch to the △ delay mode. This mode is enabled by rotating the TRACE SEP control out of the OFF position. If you are in the alternate-sweep display mode, you will now have three traces on-screen—the main sweep and two delayed sweeps. The main sweep will have two intensified zones (fig 2). The delay time to the first zone is selected by the DELAY TIME control, and the additional delay to the second zone by the △ TIME control. The time difference between the start of the two zones is digitally computed and displayed on the bottom line of the crt. The △ time readout always shows the time difference between the start of the two delayed sweeps. Internal circuitry prevents positioning the start of the second delayed sweep off-screen to avoid ambiguous △ time readings.



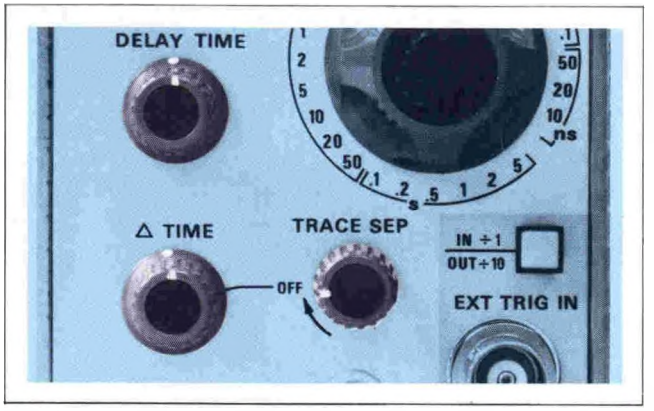



**Fig 1.** The traditional Delay Time Multiplier control is replaced by the DELAY TIME and Δ TIME controls. The TRACE SEP control enables the Δ time feature and provides trace separation of the delayed sweeps.

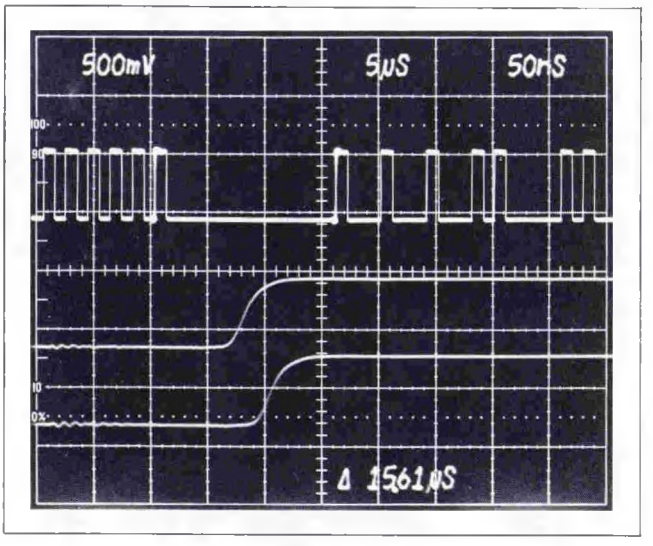



**Fig 2.** The Delaying sweep and both delayed sweeps are displayed in the Δ Time Alternate Sweep mode. Time difference between the two delays is digitally displayed at the bottom of the screen.

### Accuracy

The accuracy of Δ time measurement is specified as 0.5% of reading, ±0.03% of full scale, plus one least significant digit (full scale is 10X main sweep Time/DIV) on main time base settings from 20 ms/div to 100 ns/div.

The crt readout gives four-digit resolution for every delay time measurement, so better accuracy is achieved for time intervals approaching the full display width of the crt. For example, let's compare the accuracy when measuring the time between pulses two divisions apart with that for pulses eight divisions apart. The pulses are being displayed on a 1 ms/div sweep. The time between the pulses two divisions apart is 2 ms ± 0.0131 ms for an accuracy of 0.65%. The time between those eight divisions apart is 8 ms ±0.0431 ms for an accuracy of 0.54 %.

The accuracy of Δ time measurement is enhanced by the ability to superimpose the start and stop waveform segments for precise alignment. And the ability to view both the main and delayed sweeps while making the measurement ensures that the intended interval will be measured.

### Other features

The 7B80 and 7B85 offer several other features worth noting—1 ns/div fastest sweep rate, 400-MHz trigger bandwidth, and peak-to-peak automatic triggering. Variable trigger hold-off permits stable displays of complex signals like digital data trains. And an optional X-Y mode for the 7B80 routes the X (horizontal) signal from the oscilloscope's plug-in vertical amplifier trigger path, to the horizontal amplifier for convenience in making phase relationship measurements.

The circuitry in the 7B80 and 7B85 represents a substantial step forward in value engineering. The improved performance of the 7B80 was achieved with no increase in cost over its predecessor, the 7B70, and the Δ delay capability was included in the 7B85 with just a very modest increase. The component count and number of circuit boards were reduced considerably with an attendant improvement in reliability and ease of servicing.

### 400-MHz triggering

Two new Tek-developed ICs are key elements in achieving the 400-MHz triggering bandwidth. The first IC performs the dual function of interfacing the ECL trigger circuitry to the various trigger input paths and providing for peak-to-peak automatic operation. This versatile triggering mode permits viewing different signal levels without readjusting the triggering controls, yet maintains trigger level control for those applications where it is beneficial. Peak-to-peak automatic triggering is achieved with new techniques that eliminate double triggering, which sometimes occurs when large signals containing noise are being viewed.

The second IC contains proprietary high-speed ECL circuitry that allows the time base to trigger to 400 MHz. This IC takes the signal processed by the input IC and the holdoff signal from the last sweep and generates a gate for the next sweep. Trigger slope selection and a free-run mode are also included.

### The sweep generator

The method of sweep generation employed in the 7B80 and 7B85 is noteworthy because of its departure from the traditional Miller integrator technique. A novel gating circuit, combined with a selectable timing current source and grounded timing capacitors, give exceptionally clean sweep start characteristics over a $10^9$ to 1 range of sweep rates (fig 4). Fast sweep speed linearity and accuracy is achieved without the use of ultrahigh bandwidth integrators and their potential

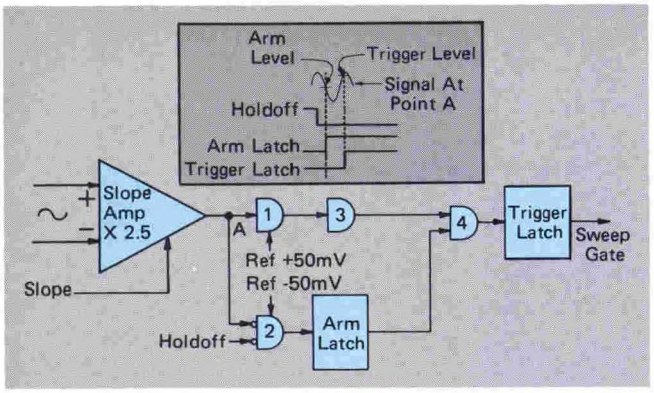



**Fig 3.** Simplified block diagram of the trigger IC. The trigger signal passes through the Slope Amplifier with a gain of ≃ 2.5 to point A. After hold-off goes low and the signal at point A passes the reference −50 mV in the negative direction, Gate 2 sets the Arm Latch, which enables Gate 4. When the signal goes back positive through the reference +50 mV at Gate 1, it propagates through Gates 1, 3, and 4 to set the Trigger Latch, which starts the sweep.

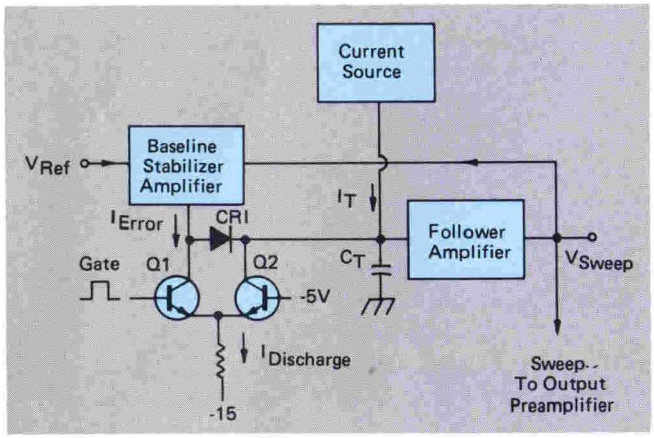



**Fig 4.** Simplified block diagram of 7B80 Sweep Generator. Prior to gating, Q1 is off and Q2 conducts allowing $C_T$ to discharge through Q2 until $V_{SWEEP}$ equals $V_{REF}$. $I_{ERROR}$ then equals ($I_{DISCHARGE} - I_T$) and flows through the forward biased diode, CR1. After gating, Q1 conducts and turns off Q2. $I_{ERROR}$ is diverted from CR1 and Q2 over to Q1, allowing $I_T$ to charge $C_T$. CR1 turns off cleanly because of the current mode nature of Q1 and Q2.

stability problems. Because of the clean response of both the ramp generator and the sweep preamplifier, only one fast timing adjustment is necessary to calibrate all rates faster than 100 ns/division. All other adjustments are performed at relatively slow sweep rates, which ensures excellent consistency from unit to unit.

An additional advantage of the 7B80 method of sweep gating is the precise control of the baseline stabilizer loop gain characteristics. Dominant pole frequency response is obtained independent of the value of the timing capacitor or the timing current. Residual baseline noise is kept to a minimum in this fashion yielding very low delay jitter (1 part in 50,000) for the delaying time base. Other types of response can lead to resonances which enhance some of the noise component frequencies, thereby causing inferior delay jitter performance.

X10 magnification is obtained by gain switching the output preamplifier. Annoying thermal shifts in position when the magnifier is switched in or out are significantly reduced with the circuit shown in figure 5. The addition of two current-follower transistors maintains a small and constant voltage across the conventional differential pair of transistors. This reduces changes in their power dissipation with changes in signal conditions and maintains a constant loadline with changes in positioning voltage.

The 7B80 and 7B85 offer calibrated sweep rates from 1 ns/div to 5 s/div in the usual 1-2-5 sequence. The Variable control extends the slow end beyond 12.5 s/div for over a "decade of decades" total range. Displayed sweep accuracies within 1.5% over the +15°C to +35°C range are available with most of the sweep rates. The 7B80 family of time bases are compatible with all currently produced and most older mainframes, and the △ delay feature of the 7B85 can be used with other 7000-Series Time Bases.

### Generating △ delays

Figure 6 shows a simplified block diagram of the circuitry used to achieve △ delay time measurements. In making delay time measurements from the point of sweep initiation, only the DELAY TIME control is used. The voltage from the DELAY TIME control, buffered by a X1 amplifier, is supplied to the First Delay Pickoff Comparator and routed to the DVM. This voltage ($V_{DELAY\ 1}$) determines the point on the main sweep at which the delayed sweep will start and the digital time readout to be displayed on the crt.

In the △ Time mode, the buffered voltage ($V_{\triangle DELAY}$) from the △ TIME control is summed with $V_{DELAY\ 1}$ to obtain $V_{DELAY\ 2}$, the voltage equivalent to the second delay. This voltage is routed to the Second Delay Pickoff Comparator, which is activated alternately with the First Delay Pickoff Comparator when operating in the △ Time mode. In this mode, $V_{\triangle DELAY}$ serves as the input to the DVM. The digital delay readout on the crt then corresponds to the delay difference.

The summed output voltage ($V_{DELAY\ 2}$) is prevented from exceeding ≃ 4.8 volts by the Second Delay Clamp, which decreases $V_{\triangle DELAY}$ as necessary. Thus, the second delay never starts off-screen and the digital readout remains correct for the entire range.

### The DVM

Using a digital voltmeter for indicating delay time or △ delay time readings gives the user accurate delay measurements without his needing to read a calibrated dial and make calculations. The heart of the DVM is a Tek-made IC containing a 4-decade counter, latches, and an encoder to output to 7000-Series mainframe crt readout circuitry.

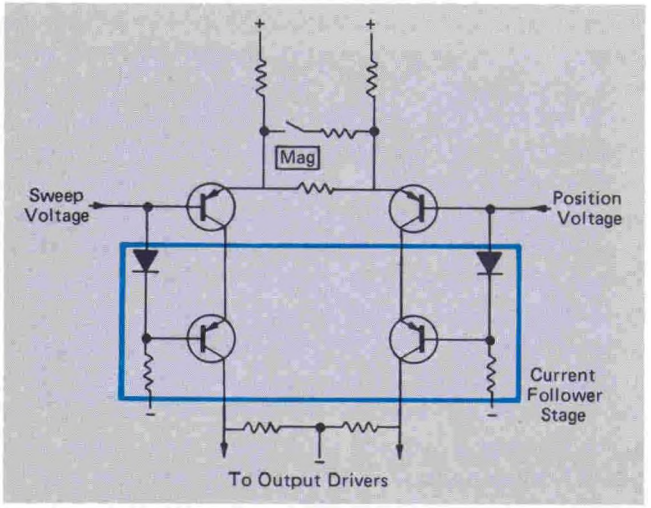



**Fig 5.** Simplified schematic of the 7B80 output preamplifier. Circuit significantly reduces shifts in position due to thermal effects when X10 magnifier is switched in or out.

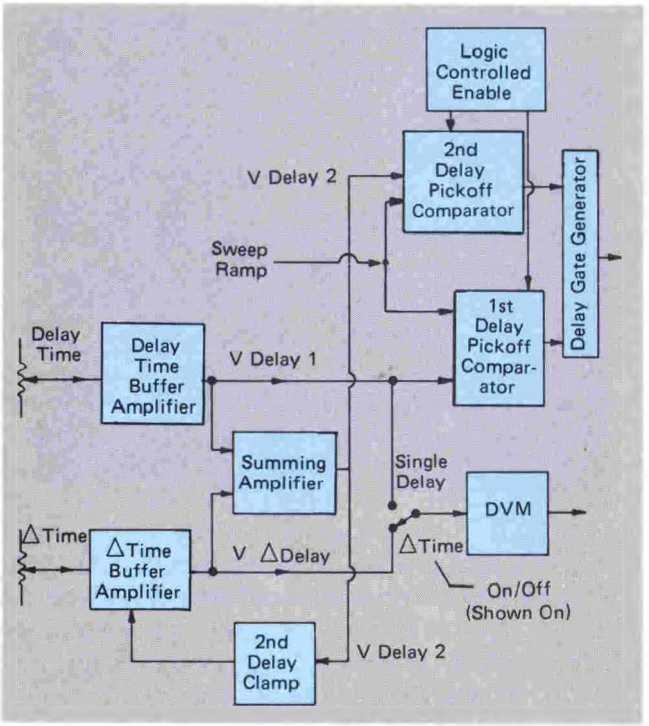



**Fig 6.** Simplified block diagram of △ delay circuitry. In a △ TIME mode, delay comparators are alternately enabled causing delayed sweep to start after respective delay is selected.

The DVM measures a $V_{DELAY}$ voltage equivalent to the delay time. The delay time is the time for the sweep ramp to reach the $V_{DELAY}$ level in the comparator. Although a change in the sweep reference voltage changes the ramp, and hence the delay time, the sweep reference also serves as the DVM reference, so that any fluctuation in its value causes both the delay time and the DVM delay time readout to change equally. This independence of voltage reference stability avoids a limitation common to most DVMs.

### Logic and trace separation

The logic for displaying delay and △ delay times is complicated somewhat by the Alternate or Chopped Horizontal modes featured in the 7000 Series. The holdoff signal generated at the end of every sweep of the 7B85 is used for switching between delaying and delayed sweeps and between first and second delayed sweeps. A divide-by-two circuit allows only every other holdoff pulse to pass to the mainframe and, at the same time, switches between pickoff comparators with every holdoff signal. This produces the following display sequence when the instrument is operating in the △ Time Alternate-Sweep mode:

1. Delaying sweep displayed with the first delay indicated by a brightened zone.
2. Delaying sweep displayed with the second delay indicated by a brightened zone. This sweep overlays the first trace so that the display appears as a single trace with two brightened zones.
3. Delayed sweep corresponding to the first brightened zone on the delaying sweep.
4. Delayed sweep corresponding to the second brightened zone on the delaying sweep.

The same divide-by-two signal that controls the holdoff output and switches between comparators also provides a signal to the trace separation circuitry. This divide-by-two signal, along with the mainframe logic signal indicating which time base is being displayed, switches a vertical axis offset signal. With the front-panel TRACE SEP control on the 7B85, the two delayed sweeps can be overlapped or separated by up to three divisions.

### Summary

The 7B80 and 7B85 offer a substantial improvement in measurement capability for the 7000-Series Oscilloscopes, particularly the 7700, 7800, and 7900 Series. The two time bases feature △ delayed time measurements, 1 ns/division fastest sweep rate, 400-MHz trigger bandwidth, and peak-to-peak automatic triggering. A sizable reduction in the number of components, circuit boards, and calibration adjustments improves reliability and ease of servicing, and results in low acquisition and ownership cost.

### Acknowledgments

Les Larson developed the trigger circuitry and served as Project Manager for the 7B80 and 7B85. The sweeps were designed by Bruce Hofer and the DVM and related logic by Paul Farley. Much credit is due Art Metz for his work on the trigger input IC which includes the peak-to-peak automatic trigger circuitry. Gene Andrews, Program Manager, provided overall direction for the project. Our thanks also to the many others who made valuable contributions to the project.

1. See "Time Measurement Accuracy," Mar/Apr 1975 Tekscope.

Abraham Taghioff

# Spotlighting hidden pulses

Narrow noise pulses, or other short duration "glitches", often cause the faulty operation of digital circuits. They may be caused by radiated noise, power line coupled noise, sliver pulses due to timing-skew input signals to gates, or other undesired circuit operations. Finding these fleeting transients can be a frustrating job, even when you know they are present. If you only suspect they are there, it is like chasing a black cat in the dark.

When pulses occur at a low rep rate, even most fast writing-rate oscilloscopes do not produce a display viewable in normal lighting conditions. A storage oscilloscope like the TEKTRONIX 7633 or 466, with fast writing-rate, easily displays these elusive pulses. By knowing where to trigger and how to operate to get the fastest storage, you can find and capture these pulses in a matter of

seconds. You should, therefore, not think of storage as merely a method of capturing one-shot events.

To illustrate this technique, we generated a pulse about 25 ns wide, and hid it in the middle of a pulse train containing pulses about 250 $\mu$s wide. The pulse trains recur about 15 times a second. Wide pulses are easily displayed, whereas the 25 ns pulses are only 1/10,000 as wide as the 250 $\mu$s pulses, and can't be seen on a 0.5 ms/div sweep. Sweeps much faster than 0.5 $\mu$s/div start to fade from view when triggered only 15 times a second.

To locate a narrow hidden pulse on a slow sweep, you put the scope in the NON STORE mode and use the triggerable-after-delay mode with the A sweep intensified by the B sweep. Observe the position of the bright zone in the trace as delay is increased with the DELAY TIME MULTIPLIER (figure 1). With this display, the beginning of the bright zone represents the instant when the delayed B sweep (set for a much faster rate than the A sweep) is triggered. The end of the zone represents the instant when the B sweep is completed and may be stored. To store the trace as soon as possible, the A TRIGGER HOLD-OFF switch should be set to B ENDS A. This stops the delaying sweep (A) as soon as the delayed sweep (B) has produced a trace. Storage then occurs immediately.

The beginning of the zone jumps from one trigger point to the next as the delay is increased, when the B sweep is delayed and triggered in the NORMAL mode. Anytime the zone jumps to a point in the display where you can't see a trigger signal, it tells you a trigger signal is there just the same (figure 2). The beginning of the bright zone in figure 1 jumped from edge to edge of each of the four preceding pulses as the DELAY TIME POSITION control was rotated. With a little more rotation, the zone jumped to the position shown in figure 2 where no pulse or pulse edge can be seen. The zone indicates where the hidden pulse resides.

Switching the horizontal display mode to view the fast delayed sweep (B) you see the display pictured in figure 3. The trace is not visible as the trigger repetition rate is too low to produce a visible trace at this fast sweep rate. This is where fast storage comes into play. By simply pressing the FAST storage button, the hidden pulse is displayed as in figure 4.

Spotlighting hidden pulses is just one of many applications for fast storage. You'll find it useful in solving many other measurement problems.

Note: The TEKTRONIX 466 was used in preparing this article. Controls on the time bases used with the 7633 differ from those on the 466, but the technique is essentially the same.

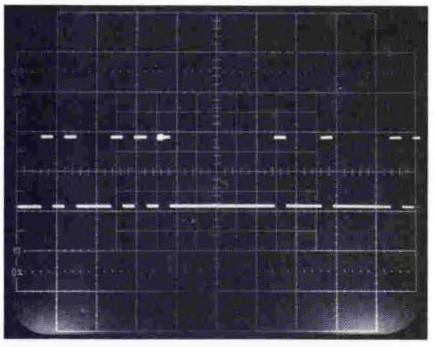


**Fig. 1.** A sweep at 0.5 ms/div intensified by B sweep gate following fifth positive-going transition.

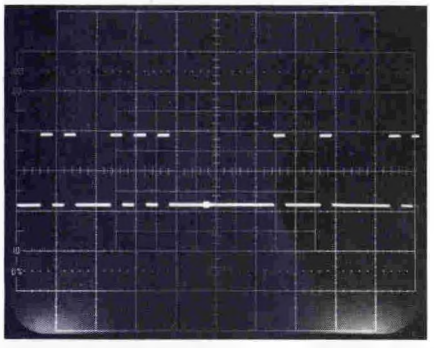


**Fig. 2.** Same display as above except DTM has been rotated slightly and B sweep is triggered on next signal, which is too narrow to be seen at 0.5 ms/div.

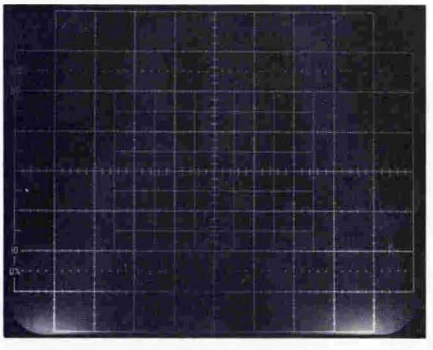


**Fig. 3.** B sweep at 50 ns/div, triggered on narrow pulse not visible in figure 2. Pulse repetition rate is too low for visible trace at 50 ns/div.

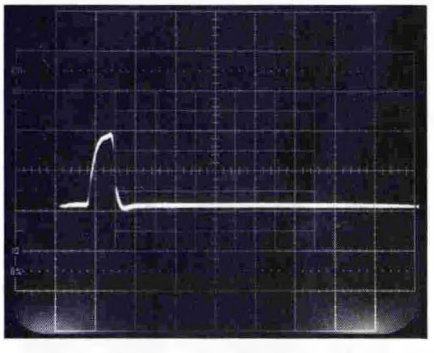


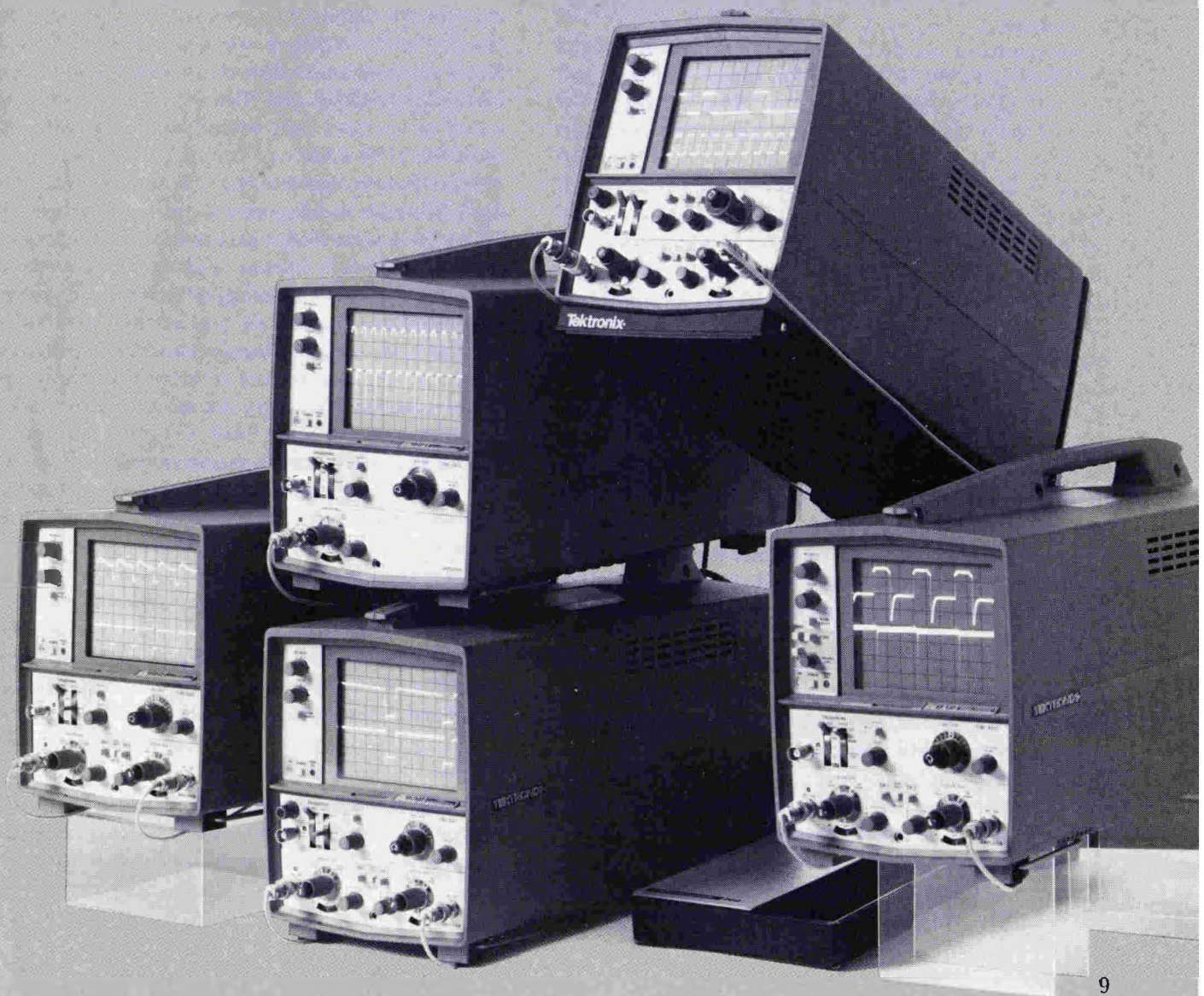
**Fig. 4.** B sweep at 50 ns/div using FAST storage. Shows 25 ns pulse not visible in figure 2 or 3.

Jim Hinze

# The T900 Series—solving the cost vs quality question.

Committed to technical excellence. That phrase has been an integral part of the Tektronix logo for many years. And it has been more than just a part of our logo—it has been our guiding philosophy in the design, manufacture, marketing, and servicing of every Tektronix product.

These remarks preface a question of great import to both Tektronix and you, the customer. There was a growing need for a basic performance, rela-



tively low cost, general-purpose oscilloscope suitable for service, production line, and classroom applications. Tektronix needed to meet that need. But could we, as a company dedicated to developing high-technology products, develop an instrument for the low-cost market without compromising our image as a builder of quality products? It was a difficult question, and one which presented a new kind of challenge to engineers accustomed to designing state-of-the-art instruments. The challenge proved to be not only interesting, but rewarding beyond our earliest expectations.

### The design goals

After carefully considering the specifications and functions needed for the various application areas, it was decided that a series of instruments, rather than a single product, afforded the best prospect for meeting the performance and price targets. As a result, it was proposed that five completely new oscilloscopes—the T900 Series—be developed. Included in the series would be two 15-MHz instruments, one single and one dual trace; two 35-MHz, both dual trace with one having delaying sweep; and one 10-MHz, dual trace, bistable storage instrument.

Measurement accuracies for both time and amplitude were to be 3% or better. This meant both low and high voltage supplies would have to be regulated. A vertical delay line was to be included for fast rise time measurements, and a big, bright crt was mandatory for many of the anticipated applications. The instrument should be highly portable for service applications and the front panel should be color-coded for easy operation by relatively inexperienced personnel. The instrument should also be highly reliable to give the customer maximum serviceability and to minimize warranty expense. An additional goal was to provide low-cost storage operation for mechanical and other low-frequency application areas.

Since Tektronix quality and reliability were to be maintained and full after-sale support provided for these products, only two major areas remained where cost savings could be realized—the number of components to be used, and the labor expended in producing and assembling those components into the finished product. Both received equal emphasis. A major key to reducing the componentry was the selection of the T4655 crt for use in the T900s. Widely used in other Tek instruments, this crt required only a fraction of the deflection voltage needed by crts used in most other low-cost instruments. This could yield a substantial reduction in amplifier components, power consumption, and heat dissipation hardware. Figure 1, showing the simplicity of the T935 vertical output amplifier, graphically illustrates the point.

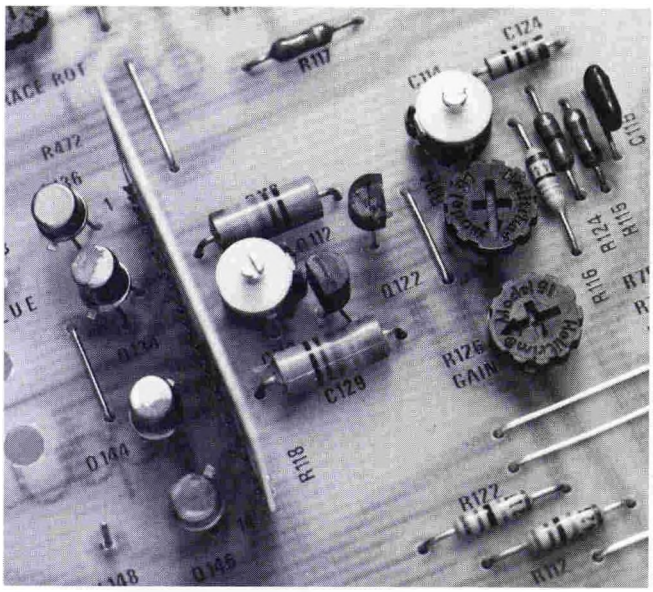



**Fig 1.** Use of a mesh crt in the T900 simplifies the driving circuitry as shown by this photo of the T935 vertical output amplifier.

Historically, Tektronix has developed and produced many of the components needed to achieve the performance we were seeking. Cost was always an important consideration but performance was the primary factor. For the T900s it was decided that off-the-shelf ICs, transistors, and other components would be used whenever possible, and Tektronix-made components would be specified only when better cost/performance ratios could be achieved.

Close liaison between engineering and manufacturing in the early development stages revealed many areas where innovative design of Tek-developed components could substantially reduce instrument assembly time. The power transformer is a good example. It is typically time-consuming to install because of the number of leads to be dressed in place, trimmed, and soldered. In the T900s, the transformer is designed so the terminals can be soldered directly to the printed circuit board. A big time saver.

Switches were another lucrative source of economy. Tek-invented cam switches provided superior performance but were time-consuming to install. A new method of capturing the cam switch contacts shortened assembly time considerably and make future servicing easier. A new design for the printed circuit board switches used for the time/division control yielded similar results. Even the front-panel control knobs came under scrutiny. The result—a molded single-piece knob and shaft (fig 2) saves time both in producing the component and installing it. This story can be repeated over and over for many components.

### Circuit design considerations

Several challenging goals faced the circuit design team: reduce the component count, shorten calibration time,

**Fig 2.** Knob and shaft are molded in a single piece to minimize production and installation times.

maximize reliability, etc. We've already mentioned the circuit economies achieved by selection of the appropriate crt. Further reductions were achieved by the simple expedient of omitting those functions usually included on more sophisticated oscilloscopes but not considered essential for the intended applications. Calibration times were shortened by designing broad tolerance circuits to eliminate adjustments, reduce the sensitivity of adjustment, and minimize the interaction between adjustments. These efforts resulted in calibration times for the T900s that are typically one eighth that of other products in volume production.

Circuits were also designed to reduce the number of front panel controls by performing some functions automatically. For example, chopped or alternate dual trace operation of the vertical amplifier is automatically selected by the time/division control. A similar function is performed for the tv triggering mode to achieve an optimum display at tv line or frame rates. A double-barreled benefit results—less expensive to produce, easier to operate.

Engineers can't resist adding a few niceties to the necessities and since the T900 designers are no exception, there are some niceties included in the T900s. The automatic operations mentioned above are examples. Another is the flashing power light that indicates when the line voltage is out of range for power supply regulation. And a beam finder is included for those times when the trace is off-screen and you wonder where. An anti-jitter circuit in the sweep provides stable displays for those instances when trigger hold-off ends just as the next trigger occurs. These and other features add much to the convenience and usability of the T900s and little to the cost.

### Mechanical design

The mechanical design team contributed their share of cost-saving techniques to the project. A major economy factor is the commonality of subassemblies. All five instruments have identical structural cores, identical outer cases, and with the exception of the storage model, identical power supplies. Almost all hand-wired connections are eliminated by generous use of etched circuit board connectors.

The two-piece, lightweight, impact resistant case molded from Cycoloy KHP material provides structural strength to the package and obviates heavy internal support structures. Portability is enhanced by the carrying handle which is an integral part of the case.

Let's take a moment to remove the case and take a look at the interior construction of the T900s. Inside we see quality single-sided etched circuit boards with surprisingly low component density. Very little cabling is evident; most boards interconnect directly. A glance at the rear of the front panel shows nothing like the usual jumble of wires. No potentiometers or switches are mounted there, either—they're all on the circuit boards. The unit appears to be easy to disassemble, and it is. For example, the vertical amplifier board, including attenuators and input connectors, is removed by taking out just three screws and lifting the assembly free from the interface board. The other boards are equally easy to remove.

### Ensuring reliability

You will recall high reliability was one of the prime design goals. Rugged construction and conservative circuit design are two positive steps toward that goal, but what else could be done? Someone suggested preconditioning all active devices. Another, an extended burn-in cycle for the entire instrument. First reaction to both suggestions was that they would be expensive. However, a thorough discussion of the savings to be realized in reduced production and warranty costs due to fewer component failures culminated in a decision to implement both steps. As a result, all active components in the T900s are preconditioned and pretested. Figure 4 shows a portion of the component preconditioning equipment. All T900s also undergo a 7-day burn-in cycle at an elevated temperature. Figure 5 pictures that activity in process. Early results indicate both programs are paying dividends.

### Economies in production

Thus far we haven't said much about economies in production aside from those achieved through component design and commonality of sub-assemblies. Substantial economies are also effected through machine insertion of components. (About 70% of the components are machine inserted, compared to ≈40% for the typical instrument). Large, standard-sized circuit board flats are used to achieve maximum efficiency from the insertion machines and to minimize handling. These large boards are later divided into individual circuit boards, hand inserted parts are installed, and the board is flow sol-

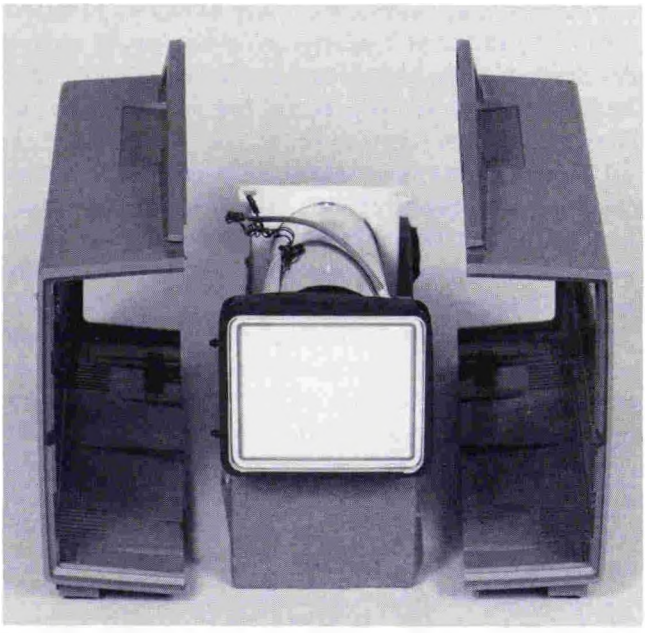


**Fig 3.** The structural core and outer case are common to all T900s. Commonality of subassemblies reduces cost.

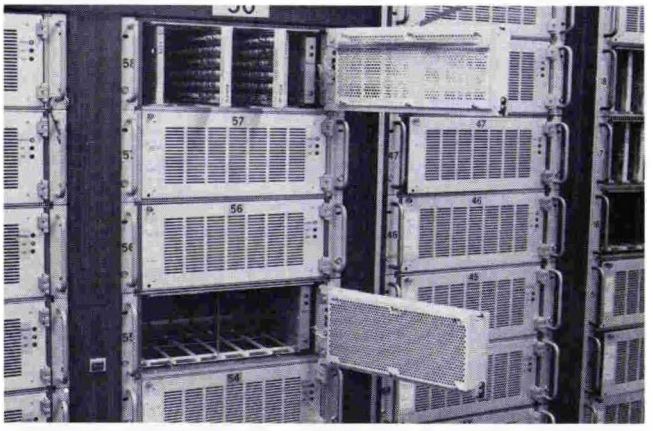


**Fig 4.** A portion of the transistor power cycling equipment used in preconditioning T900 active components.

**Fig 5.** Partial view of cycle rack where T900s undergo 7-day burn-in cycle at elevated temperatures.

dered. The boards are then machine tested before installation in final assembly. The entire instrument undergoes the 7-day burn-in cycle before final calibration takes place.

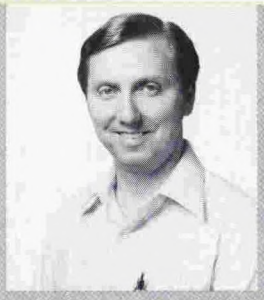
### Accessories are important

All of the efforts expended to bring you a line of reliable, quality, low-cost instruments would fall short, unless accessories were provided to let you fit these new products to your particular application. Probes, of course, are the most important accessory for oscilloscope users. They are included as standard equipment with the T900s, and so are comprehensive instruction manuals with complete operating and servicing information.

A full complement of optional accessories is available for your special needs. A lightweight scope stand holds the T900 at an angle convenient for viewing and gives you easy access to controls. The stand can be quickly disassembled and attached to the bottom of the scope for easy carrying. A new low-cost camera, the C-5A, attaches directly to the front panel of the T900s without adapters, uses Polaroid pack film, and provides graticule illumination. Front-panel covers protect the controls during transport or storage and have room to store two probes and other accessories.

### The project team

Designing and producing the T900 Series has been a new and exciting experience for those of us associated with the project. Jim Hinze, project manager, headed the team consisting of Mike Cranford, Al Hill, Jaime Navia, Lee Jalovec, Pete Janowitz, Scott Jansen, Dave Laib, Bert tenKate, Jim Proebstel, Tom Schaper, Bill Glaze, and Bob Hartman. Our thanks to the many others who provided valuable inputs and assistance.



Don Hall

# A 50-MHz pulse generator with variable transition times

Pulse generators have traditionally been general-purpose instruments designed to cover a broad range of test applications. Today's abundance of logic families, each with its own unique test requirements, has created even more demands on pulse generator performance. The PG 508 50-MHz Pulse Generator is specifically designed to provide basic capabilities for this broad applications base.

An output of 20 V peak-to-peak into a high impedance (10 V into a 50-Ω termination) over a ± 20-V dynamic range makes the PG 508 compatible with MOS circuitry. And the 5-ns variable leading and trailing transition times accommodate TTL or ECL applications. Several unique features simplify control setup, making the PG 508 faster and easier to use than earlier generation instruments.

## Versatile triggering or gating

Unusual flexibility is available when the PG 508 is gated or triggered. A FET input buffer stage, which allows for the selection of 50-Ω or 1-MΩ input im-

pedance, provides a clean termination for high-frequency triggering signals or negligible loading on high-impedance logic circuits. Thus the PG 508 may be triggered from any point in a logic circuit without degrading system performance. A trigger slope polarity switch and trigger level control provide additional flexibility for external timing control.

Stable triggering or gating requires only an 80-mV signal (250 mV for frequencies above 10 MHz) within a ±3-V dynamic range. An oscilloscope probe may be used with the 1-MΩ input to access signals directly or to increase the trigger level range by the attenuation factor of the probe. These features virtually eliminate the need for special interface circuits.

A unique indicating scheme simplifies the procedure for external triggering or gating. A three-state logic circuit drives an LED so that, with positive slope selected, the LED is OFF continuously below threshold, ON continuously above threshold, and flashing for repetitive triggering. This feature allows the PG 508 to be used as a logic probe.

The external gating function is ideal for logic testing in which a controlled number of pulses are required. Synchronous gating – starting the first pulse at gate initiation and completing the last pulse in progress – prevents counting errors in the logic system under test. In the "counted burst" mode the PG 508 can be used with the TEKTRONIX DD501 Digital Delay to provide a precise, thumbwheel-selected number of pulses regardless of the start pulse duration or PG 508 repetition rate.

A pushbutton for triggering single pulses manually is a standard feature on many pulse generators. The PG 508 includes this feature and has the added capability of manually triggering pulse bursts in the synchronous gate mode. The user can change the slope selection by pushbutton to gate the generator *off*. The pulse generator thus becomes a convenient source for long pulse trains useful in testing divide-by-n counters.

Another useful mode, external duration, converts the PG 508 from a pulse generator to a pulse amplifier. In this mode the TRIG/GATE input signal can be converted to an output signal with the full output capabilities of the generator, including variable leading and trailing transition times. The instrument can then be used as a pulse conditioner to interface directly between circuits or logic families of different voltage levels, transition time capabilities, or impedance levels.

The trigger output is another example of innovative design in the PG 508. Instead of the short duration trigger used by many pulse generators, the trigger output is a square wave, ensuring compatibility and ease of use with lower speed logic families and circuits. The + TRIG OUT can be complemented simply by changing an internal cable connection.

**Variable transition and delay times**

Sophisticated pulse generators like the PG 508 include delay and transition timing control in addition to the basic timing functions of period and duration. The delay function provides timing control for designing and troubleshooting logic, radar, process control, and other systems requiring variable timing between events. During double pulse operation the delay circuitry controls the pulse separation timing. The double pulse mode provides a quick method for checking the resolution and recovery characteristics of circuits by reducing the interpulse spacing until the test circuit fails to resolve the two pulses.

The variable transition timing function in the PG 508 provides close test simulation of circuit parameters. Analog application tests such as amplifier slew rates and comparators, or logic performance tests such as CMOS (where power increases with decreasing transition times) are easily performed. In the PG 508, the leading and trailing times remain constant with changes in the output amplitude, thereby reducing instrument setup time. Independent leading and trailing transition time adjustments (100:1 vernier controls with decade ranges) greatly increase the versatility of the pulse generator for nonpulse applications like generating ramps or simulating signals with unequal slew rates.

**Customizing your pulse generator**

Each of the four timing functions – Period, Delay, Duration, and Transition Time – includes a custom timing position, a feature unique to TEKTRONIX generators. The addition of a user-selected capacitor provides an extra low-speed timing range or a known repeatable setting which doesn't require the adjustment of variable controls.

Setting up timing controls is further simplified by the square wave mode, which produces a 50% duty cycle output for any period setting.

**Control Error Indication**

The increased timing functions available in the more sophisticated pulse generators can create setup problems. Well-known to most users is the familiar frequency division of pulse output caused by setting a delay or duration greater than period. However, if the transition time is adjusted to greater than the duration or period, there is an even more insidious result – no pulse output at all. Other illegal setup modes can produce similar no-output conditions, or modes of operation where front-panel controls do not correctly define the output pulse.

The PG 508 is the only generator on the market that warns the operator of these hazards. A three-state logic LED circuit is again employed. A steady ON indicates that an improper mode has been selected – for exam-

ple, external duration with an internal period. The indicator flashes for timing errors such as transition time exceeding duration; the indicator is OFF for normal operation where the output is correctly defined by the control settings.

### Output innovations

The output section of the PG 508 contains its share of innovations. Basically, the output amplifier functions as a voltage source behind a 50-Ω source impedance. The 20-V peak-to-peak output with a ±20-V dynamic range into an open circuit (10 V peak-to-peak, ±10-V dynamic range into 50 Ω) is ideally suited for MOS applications, and is applicable for driving all types of logic currently being produced in large quantities.

The 50-Ω source impedance has a low reactive component, providing minimum abberations for signals delivered to reactive loads or at the end of unterminated cables. This allows the operator to use transition times to 5 ns without a terminating load.

Provision is made for selecting either pulse "normal" or pulse "complement" modes with a single front-panel pushbutton. This feature can be used to obtain duty cycles greater than 99%.

Logic parameters are specified relative to threshold levels rather than to the amplitude and offset levels provided by some pulse generators. The PG 508 provides independent high and low level controls and has the ability to obtain minimum pulse amplitude anywhere within the ±20 V dynamic range of the output. Thus logic characteristics that are a function of an individual level can be evaluated quickly and accurately. An external level monitor provided through the rear interface can be used to set high and low levels accurately with a DVM. This can be quickly accomplished by pushbutton on TM 500 DVMs which have a rear interface external input.

The PG 508 is the only pulse generator on the market with the convenience of preset output levels. Just a push of the PRESET button changes the output from variable high and low level control to screwdriver-adjustable

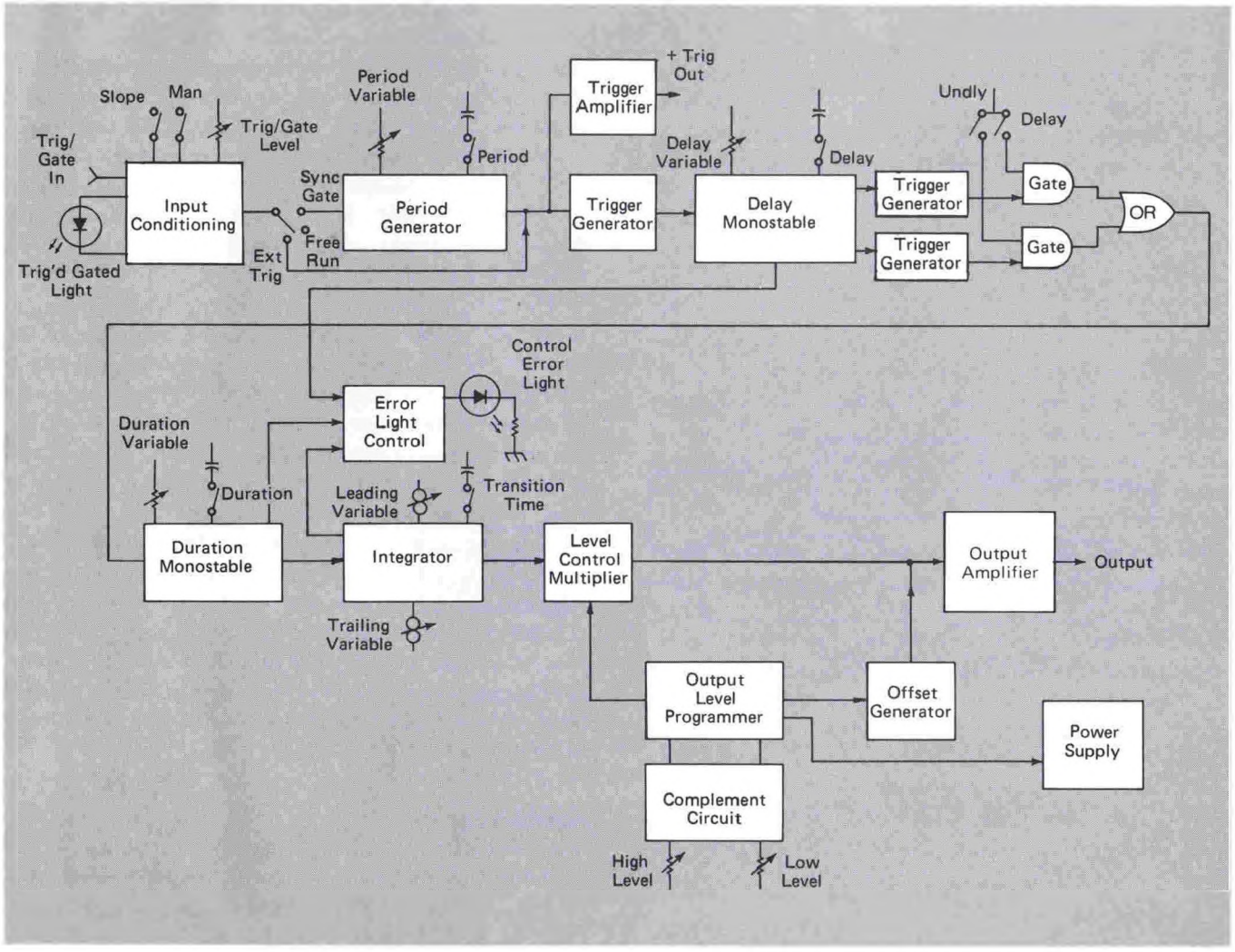



**Fig 1.** Simplified block diagram of the PG 508 Pulse Generator.

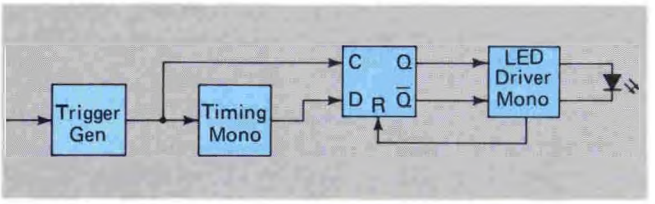



**Fig 2.** Simplified block diagram of the error light control circuit which monitors all timing functions and provides an indication when illegal modes or improper control settings are selected.

preset levels. This feature helps avoid spending time setting up logic test levels repeatedly. It also helps avoid accidental changes in output levels which could inadvertently damage circuits under test. This is especially important for CMOS logic, where 0.3 V above supply potential can typically cause permanent damage. In system or dedicated applications the PG 508 output levels can be programmed to track external voltage inputs applied to the rear interface connector. This provides safe, fast setup by using system power supplies as level control voltages.

### Block diagram discussion

A block diagram of the PG 508 is shown in figure 1. The design for Period, Duration, and Delay takes advantage of the technology developed for the PG 502 250-MHz Pulse Generator. This approach uses 10K series ECL to provide a low-cost, high-speed method for achieving the timing functions while maintaining a constant power supply loading for the best system performance and clean transient response.

The Error Light Control circuit and the Level Control Multiplier are new concepts developed for the PG 508. The Error Light Control circuit monitors all timing functions and indicates the selection of illegal modes or improper control settings. The basic element in this circuit is a D master-slave flip-flop used for differential time measurements. The D input is the timing monostable output, and the clock input is the same as the monostable trigger source.

For normal operation, the timing monostable completes the pulse before the next trigger (clock) arrives, and the flip-flop is not set. However, for excessive duty cycle settings, triggers occur before the timing monostable has completed the pulse, clocking and setting the flip-flop. This condition triggers a monostable which causes the Control Error LED to flash at a visible rate.

The Error Light Control circuit for transition time is similar. If the pulse transition is not $\simeq 50\%$ completed before the next clock pulse (the input pulse from the duration circuit), the D flip-flop will be set. The Control Error LED will flash in this case too, indicating an invalid output.

The Level Control Multiplier, Output Level Programmer, and Offset Generator provides independently variable high and low output levels. The key element in this approach is a Tek-made IC used as a four-quadrant (X-Y) multiplier. Commercially available multipliers do not have the bandwidth or transient response required for this application. The particular IC used has a bandwidth $>200$ MHz and maintains excellent transient response characteristics over a 20:1 amplitude control range. The variable transition time signal serves as the X-input, and the Y-input is the difference between the high and low level control voltages (dc) from the Output Level Programmer.

Any change in either level control voltage produces a pulse amplitude change due to multiplier action. But, the Output Level Programmer causes an offset to be generated which corresponds to exactly one half this amplitude variation. Therefore, varying an output control affects one pulse level without affecting the other.

Linearity was an important consideration in the design of the multiplier since a generator with variable transition timing requires that all succeeding stages be linear. Linear control of the amplitude and the offset generator which compensates for amplitude variations allows the PG 508 to obtain a high degree of independence between the output level adjustments. This approach also provides continuously variable gain and clean transient response, especially at low signal levels. A switch reversing the level control voltages provides the pulse complement function. Using voltages to control the pulse levels also provides a straight-forward output level preset function and allows the output levels to be externally voltage programmed.

The design constraints for the output amplifier presented the greatest challenge in the development of the PG 508. Innovative design was required to obtain a 20-V peak-to-peak output over a $\pm 20$-V dynamic range with good transient response for 5-ns transitions, while minimizing power consumption and cost. The key was separate dual power supplies for the output amplifier that track the level control voltages. With this approach, the output transistors can be operated at approximately half the voltage required by common output amplifier techniques, which results in increased reliability, higher bandwidths, and lower cost. The output section is configured as a complementary transconductance feedback amplifier that provides greater level stability and transient linearity than open-loop methods.

### Acknowledgments

Mike Reiney was Group Leader and provided overall guidance for the project. Don Hall, the author, was Project Engineer. The electrical design team included Fred Beckett, Dennis Feucht, and Tom Hill, with mechanical design provided by Gary Kersey.

John Mulvey

# Troubleshooting phase lock loops

## Servicescope

Troubles occurring in circuits using feedback can be hard to isolate. The more complex the feedback loop, the more complex the problem. But with a little understanding and the right techniques you can do a straightforward, professional job of troubleshooting such circuits.

The phase lock loop is a typical example. This circuit is becoming more and more common, so it's a good idea to have a clear understanding of how it is used and how it works.

Phase lock loops are used to control the frequency of an oscillator so that it is some precise multiple of a reference signal frequency. For example, you can use a 1-MHz crystal-controlled oscillator signal as a reference to control the frequency of a 100-MHz voltage-controlled oscillator (VCO). This gives the 100-MHz signal practically the same accuracy as the crystal-controlled 1-MHz signal.

The principles of how phase lock loops work can best be explained by first having a look at a basic block diagram (fig 1). By making the frequency divider circuits count down by a specific ratio, like 100:1, the VCO is made to oscillate at precisely 100 times the reference frequency. The output of the phase detector supplies a voltage of the right polarity and magnitude to hold the output frequency constant at that multiple. Any tendency for the output frequency ($f_o$) to change causes a change in phase between the reference signal ($f_r$) and the divided feedback signal ($f_d$). That change results in altering the frequency-control voltage, minimizing the phase change and, consequently, keeping the frequency constant.

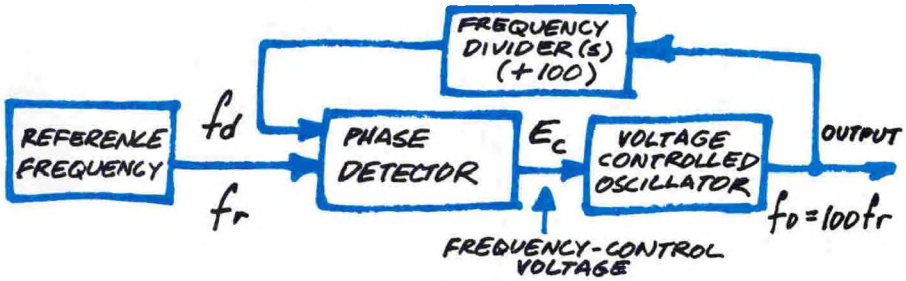



**Fig 1.** Simplified block diagram of a phase lock loop.

Before starting to troubleshoot the loop, it is helpful to identify its main signal paths on your schematic diagram. Because the reference signal and VCO output signal will usually be present even when the loop is not working, you should first check for those signals with a scope. If one is absent, the trouble is probably with the circuits surrounding the missing signal.

If both signals are present, check for the presence of the divided signal. If the divided signal is not present you should find out at what point in the divider string it disappeared. You start at the output and work back through the divider string.

If the divided signal is present, check whether it is the same frequency as the reference signal and locked to it. You can do this very simply, using a dual-trace scope, by displaying the reference signal on Channel A, triggering on the Channel A signal only, and displaying the divided signal on Channel B. If the signal on Channel B does not drift horizontally, the two signals are locked together.

When the reference signal and divided signal are synchronous and have the same frequency, the phase lock loop is probably OK. If any one of the dividers has the wrong ratio, however, the output frequency will be in error. You can check for the right divider ratio at any point in the divider string by displaying the lower frequency signal on Channel A, triggering on it, and displaying the higher frequency signal on Channel B. The ratio of the signals will be the ratio of the divider. If the ratio should be 5 to 1, but six cycles of the higher frequency signal occupy one cycle of the lower frequency signal, you know that divider is bad.

If the divided signal is present but not synchronous with the reference signal the problem can be in either the divider string or the phase detector. To determine if the divider is at fault proceed the same as if you were checking the divider ratios, but check to see whether each divided signal is synchronous with the next highest frequency signal in the string. If not synchronous, the Channel B signal will drift horizontally with respect to the Channel A signal and the trouble will be in that stage. If all divided signals are synchronous and of the proper ratio, the trouble will be somewhere in the only remaining circuit, the phase detector.

### TG501 time mark generator loop

To give you an idea of how quickly most faults in a phase lock loop can be located we will use the TEKTRONIX TG501 Time Mark Generator (fig 2) as an example. To pinpoint the problem area follow these steps and check for:

1. Signal at pin 13 of U290. If none, VCO is the problem.
2. Signal at pin 1 of U230. If none, reference signal is the problem.
3. Signal at pin 5 of U230. If none, dividers are the problem.
4. Signal at pin 5 of U230 synchronous with signal at pin 1 of U230. If not the divider should be checked.
5. Voltage at pin 2 of U250 is +2V. If not, phase comparator is the problem.
6. Voltage at pin 6 of U250 is about +7V. If not, loop amplifier (part of phase detector) is the problem.

The TG501 has an out-of-lock detector circuit which should interrupt the marker output if the VCO output signal is not synchronous with the reference frequency signal. If that circuit is faulty the output may be blocked even though the loop is OK. The collector of Q270 will be high if that circuit is faulty.

Although phase lock loops all have a lot in common, there may be some unique differences that you will occasionally encounter, such as with the out-of-lock detector in the TG501. Those circuits should be easier to identify and analyze once you understand the basic phase lock loop.

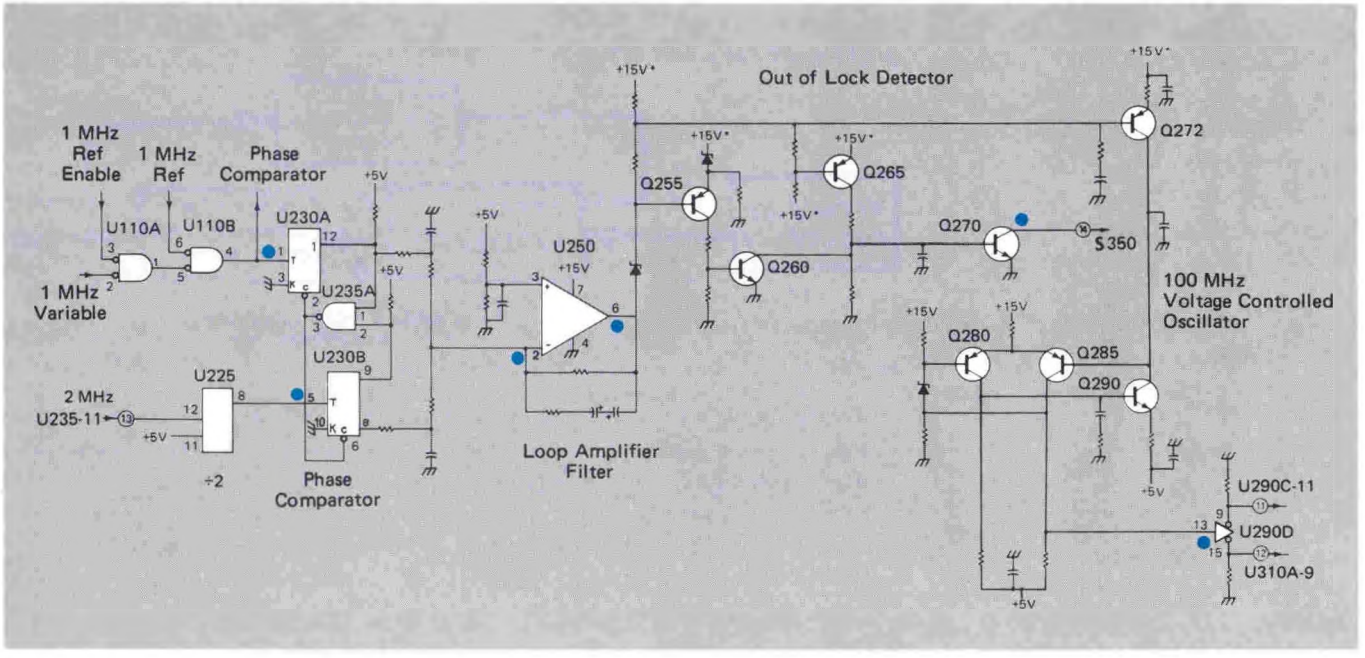
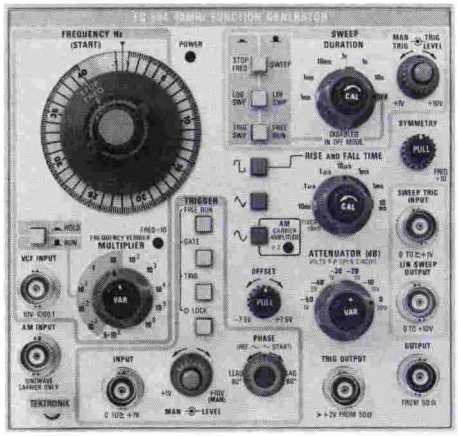



**Fig 2.** Partial schematic of the TG 501 Time Mark Generator showing key points to check to pinpoint problem area in the phase lock loop.

# New products
# New products
# New products



### 40 MHz Function Generator

The FG 504 Function Generator provides high-quality, low-distortion sine, square, triangle, ramp, and pulse waveforms. The frequency range is from 0.001 Hz to 40 MHz over nine decades (0.001 Hz to nominally 4 MHz for waveforms requiring use of variable symmetry control). An additional position for a user-determined frequency is provided.

The instrument can be swept between the START and STOP dial settings at either a linear or logarithmic rate. The output may be phase locked, gated, or triggered. A step attenuator and variable amplitude adjustment control the output amplitude over a range of 0 to 30 V peak-to-peak into an open circuit. An output offset control is provided.

### 1 GHz Leveled Sine Wave Generator

The SG 504 Leveled Sine Wave Generator is primarily intended to extend the capability of the TEKTRONIX Oscilloscope Calibration Package to 1050 MHz. It provides a constant amplitude sine wave output over the frequency range of 245 MHz to 1050 MHz in two ranges. A reference frequency of either 50 KHz or 6 MHz (selected internally) is activated by a front-panel pushbutton, enabling you to quickly check the reference level setting without changing the dial.

The output amplitude can be set over the range of 0.5 V to 3.0 V peak-to-peak by a front-panel, five-turn, calibrated control. A frequency monitor provides a convenient means to more precisely determine the output frequency by use of a counter. Provision is made to

frequency modulate the output signal over a range of dc to 100 KHz using an external source. Since this input is dc-coupled, it can also be used for remote fine frequency control.

### Versatile New Oscilloscope Cart

The Tek Lab Cart Model 3 introduces a new line of versatile, general purpose oscilloscope carts. It's top tray accommodates all three and four plug-in mainframes of 5100, 5400, and 7000 Series Oscilloscopes. It can also accommodate TM 503 or TM 504 Mainframes, portable scopes, 507, 576, and 577 instruments. The cart includes a large drawer in the base with provision for padlock, brakes on front casters, 15 ft power cord with plug strip, and safety belt.

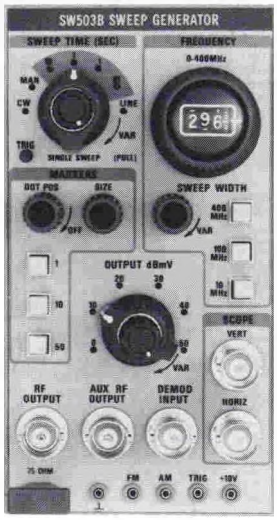
A framework attached to the underside of the tilting top tray accepts one or more shelves (one of which is standard) at any one of ten positions to permit the use of various configurations of instruments such as the TM 500 Series.

### 400 MHz Sweep Generator

The SW503 Sweep Generator is a small compact unit, which incorporates most of the features associated with larger laboratory type sweep generators, and is designed to operate in a TM 500 Series Power Module.

The instrument covers a frequency range of 1 to 400 MHz. It has a variable sweep rate, step attenuator, and a crystal controlled marker generator which provides comb type markers at 1, 10, and 50 MHz.

A unique feature of the SW503 when used in conjunction with a DC502 OPTION 7 Digital Counter is its ability to provide a variable marker over the entire 1 to 400 MHz frequency range with the marker frequency read directly on the digital counter.




### Low Cost Oscilloscope Camera

The C-5A is an easily operated inexpensive camera that will fit a broad range of TEKTRONIX oscilloscopes. It offers both graticule flash and non-flash models. Graticule flash is used with T900 and 5100 Series Oscilloscopes, and non-flash models with 434, 455, 464, 466, 475, and 7000 Series Oscilloscopes.

The f/16 lens system has a fixed focus, with customer-selectable 0.67 or 0.85 magnification for 9.76 x 12.2 cm and 8 x 10 cm displays.

### Dual Trace Portable Patient Monitor

The 414 Portable Patient Monitor is a dual-trace monitor designed to simultaneously display ECG and blood pressure or peripheral pulse. Heart rate, systolic/diastolic blood pressures, mean blood pressure, or temperature are digitally displayed for increased accuracy and convenience. Rate alarm limits are also set digitally. Because an internal battery pack permits portable operation, the 414 can be as easily used for cardiac catheterization as for surgery and recovery. All of this monitoring capability is built into a small portable package weighing only twelve pounds.

A-3321

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